SanDisk®

iNAND™ Ultra

e.MMC 4.51 I/F

Released Data Sheet
80-36-03494

Feb 2013

SanDisk Corporation
Corporate Headquarters • 601 McCarthy Boulevard • Milpitas, CA 95035
Phone (408) 801-1000 • Fax (408) 801-8657
www.sandisk.com

REVISION HISTORY

Doc. No	Revision	Date	Description	Reference
80-36-03494	0.1	6-May-12	Preliminary	
80-36-03494	1.0	Sep-12	First release	
80-36-03494	1.1	Nov-12	Update reference to eMMC 4.51 specification Updated Register values: 1. Updated POWER_CLASS to report 4GB = 0h; 9GB = 2h 2. PROGRAM_CID_CSD_DDR_SUPPORT update to 1 3. Correct S_A_TIMEOUT value 4. Update DRIVER_STRENGTH to type 0	
80-36-03494	1.2	Jan-13	1. Fixed typo in table 6 (“E” to “e”) 2. Updated SanDisk Headquarters address	
80-36-03494	1.3	Feb-13	1. Fix typo in sampling SKU	

80-36-03494.Mayy 2012 Printed in U.S.A

TABLE OF CONTENTS

1. INTRODUCTION

1.1. General Description

iNAND Ultra is an Embedded Flash Drive (EFD) designed for mobile handsets and consumer electronic devices. iNAND Ultra is a hybrid device combining an embedded thin flash controller and standard MLC NAND flash memory, with an industry standard e.MMC 4.51[1] interface.

Empowered with a new e.MMC4.51 feature set such as Power Off Notifications and Packed commands, as well as legacy e.MMC4.41 features such as Boot and RPMB partitions, HPI, and HW Reset the iNAND Ultra e.MMC is the optimal device for reliable code and data storage.

Designed specifically for mobile multimedia applications, iNAND Ultra is the most mature on board MMC device since 2005, providing mass storage of up to 128GB in JEDEC compatible form factors, with low power consumption and high performance - an ideal solution for multimedia handsets of 2.5G, 3G, 3.5G and 4G.

In addition to the high reliability and high system performance offered by the current iNAND family of products, iNAND Ultra offers plug-and-play integration and support for multiple NAND technology transitions, as well as features such as advanced power management scheme.

iNAND Ultra uses advanced Multi-Level Cell (MLC) NAND flash technology, enhanced by SanDisk's embedded flash management software running as firmware on the flash controller.

iNAND Ultra architecture and embedded firmware fully emulates a hard disk to the host processor, enabling read/write operations that are identical to a standard, sector-based hard drive. In addition, SanDisk firmware employs patented methods, such as virtual mapping, dynamic and static wear-leveling, and automatic block management to ensure high data reliability and maximize flash life expectancy.

SanDisk iNAND Ultra provides 4GB and 8GB of memory for use in mass storage applications. In addition to the mass-storage-specific flash memory chip, iNAND Ultra includes an intelligent controller, which manages interface protocols, data storage and retrieval, error correction code (ECC) algorithms, defect handling and diagnostics, power management and clock control.

iNAND Ultra enables multimedia driven applications such as music, photo, video, TV, GPS, games, email, office and other applications.

The breakthrough in performance and design makes iNAND Ultra the ideal solution for mobile handset vendors, portable navigation and Automotive Infotainment vendors who require easy integration, fast time to market and high-capacity.

1.2. Plug-and-Play Integration

iNAND optimized architecture eliminates the need for complicated software integration and testing processes and enables a practically plug-and-play integration in the system. The replacement of one iNAND device with another of a newer generation requires virtually no changes to the host. This makes iNAND the perfect solution for platforms and reference designs, as it allows for the

[1] Compatible to JESD84-B451

utilization of more advanced NAND Flash technology with minimal integration or qualification efforts.

SanDisk iNAND Ultra is well-suited to meet the needs of small, low power, electronic devices. With JEDEC form factors measuring 11.5x13mm (153 balls) form factor compatible with 0.5mm ball pitch, iNAND Ultra is fit for a wide variety of portable devices such as multi-media mobile handsets, personal media players, GPS devices and Automotive infotainment (car multimedia and car navigation).

To support this wide range of applications, iNAND Ultra is offered with an MMC Interface.

The MMC interface allows for easy integration into any design, regardless of the host (chipset) type used. All device and interface configuration data (such as maximum frequency and device identification) are stored on the device.

Figure 1 shows a block diagram of the SanDisk iNAND Ultra with MMC Interface.

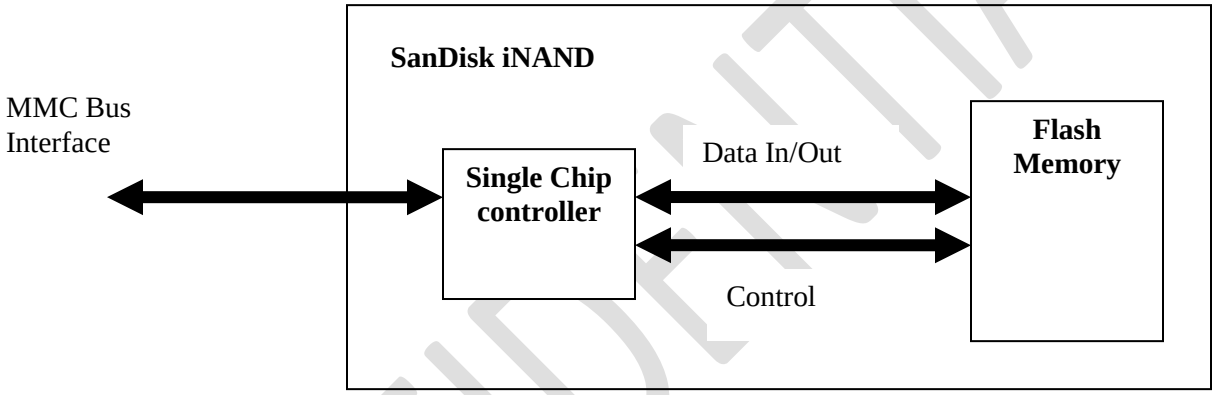


Figure 1 - SanDisk iNAND Ultra with MMC I/F Block Diagram

1.3. Feature Overview

SanDisk iNAND *Extreme*, with MMC interface, features include the following:

- Memory controller and NAND flash
- Complies with e.MMC Specification Ver. 4.51[2]
- Mechanical design complies with JEDED MO-276C Specification
- Offered in two TFBGA packages of e.MMC 4.51[3]
  - 11.5mm x 13mm x 1.0mm
- Operating temperature range: –25C° to +85C°
- Dual power system
- Core voltage (VCC) 2.7-3.6v
- I/O (VCCQ) voltage, either: 1.7-1.95v or 2.7-3.6v

[2] Refer to JEDEC Standards No. JESD84-B451

[3] Refer to JEDEC Standards No. JESD84-C441

- Up to 8GB of data storage.
- Supports three data bus widths: 1bit (default), 4bit, 8bit.
- Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed)
- Up to 104 MB/sec bus transfer rate, using 8 parallel data lines at 52 MHz, DDR Mode
- Correction of memory field errors
- Designed for portable and stationary applications that require high performance and reliable data storage

1.4. Functional Description

SanDisk iNAND Ultra contains a high-level, intelligent subsystem as shown in Figure 1. This intelligent (microprocessor) subsystem provides many capabilities not found in other types of storage devices. These capabilities include:

- Host independence from details of erasing and programming flash memory
- Sophisticated system for managing defects
- Sophisticated system for error recovery including a powerful ECC
- Power management for low power operation

1.5. Technology Independence

SanDisk iNAND *Ultra* uses 512 bytes as sector size. To write or read a sector (or multiple sectors), the host software simply issues a read or write command to the device. The command contains the address and number of sectors to write or read. The host software then waits for the command to complete.

There is no host software involvement in the details of flash operations such as erase, program or read. This is extremely important since flash devices are becoming increasingly complex with current advanced NAND MLC processes. Because iNAND uses an intelligent on-board controller, host system software will not need to be updated as new flash memory evolves. In other words, systems that support iNAND technology today will be able to access future SanDisk devices built with new flash technology without having to update or change the host software.

1.6. Defect and Error Management

The SanDisk iNAND Ultra contains a sophisticated defect and error management system. If necessary, iNAND will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume any user data space. In the extremely rare case that a read error does occur, iNAND has innovative algorithms to recover the data. These defect and error management systems, coupled with the solid state construction, give SanDisk iNAND Ultra unparalleled reliability.

1.7. MMC bus and Power Lines

SanDisk iNAND Ultra with MMC interface supports the MMC protocol. For more details regarding these buses refer to JEDEC standards No. JESD84-B451.

The iNAND bus has the following communication and power lines:

- CMD: Command is a bidirectional signal. The host and iNAND operate in two modes, open drain and push-pull.
- DAT0-7: Data lines are bidirectional signals. Host and iNAND operate in push-pull mode.
- CLK: Clock input.
- RST_n: Hardware Reset Input
- VCCQ: VCCQ is the power supply line for host interface.
- VCC: VCC is the power supply line for internal flash memory.
- VDDi: VDDi is iNAND's internal power node, not the power supply. Connect 0.1uF capacitor from VDDi to ground.
- VSS, VSSQ: ground lines.

1.7.1. Bus operating conditions

Table 1 - Bus operating conditions

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.5	VCCQ+0.5	V
Input Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA
Output Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA

Table 2 – Power supply voltage

Parameter	Symbol	Min	Max	Unit

Supply Voltage	VCCQ (Low)	1.65	1.95	V
	VCCQ (High)	2.7	3.6	V
	VCC	2.7	3.6	V
	VSS-VSSQ	-0.5	0.5	V

2. e.MMC4.51 Selected Features Overview

2.1. Discard

iNAND supports discard command as defined in e.MMC4.51 spec[4]. This command allows the host to identify data which is not needed, without requiring the device to remove the data from the Media. It is highly recommended for use to guarantee optimal performance of iNAND and reduce amount of housekeeping operation.

2.2. Power Off Notifications

iNAND supports power off notifications as defined in e.MMC4.51 spec[5]. The usage of power off notifications allows the device to prepare itself to power off, and improve user experience during power-on.

- **Latency** – overall user experience is improved. Device returns quicker from each write operation
- **Burst performance** is improved – performing housekeeping allows us to better prepare for the next burst operations. (Cleaning up the SLC cache for future usage)
- **Graceful shutdown** – power off notification itself allows the device to shutdown properly and save important data for fast boot time on the next power cycle

2.3. Packed Commands

To enable optimal system performance, iNAND supports packed commands as defined in e.MMC4.51 spec[6]. It allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus. Thus, it allows reducing overall bus overheads.

Faster sequential write performance on platform level using packed CMD

- Convert packed sequential commands to a single internal write. (ie. 8x128K packed writes become a single 1MB write)
- Hides host TAT, pipelines writes

2.4. Boot partitions Size

iNAND supports e.MMC 4.51 boot operation modes.

Boot partition size is reflected in BOOT_SIZE_MULT register value in extended CSD.

2.5. Automatic Sleep Mode

A unique feature of iNAND is automatic entrance and exit from sleep mode. Upon completion of an operation, iNAND enters sleep mode to conserve power if no further commands are received.

[4] For additional information refer to JEDEC Standard No. JESD84-B451

[5] For additional information refer to JEDEC Standard No. JESD84-B451

[6] For additional information refer to JEDEC Standard No. JESD84-B451

Typically the entrance to sleep mode occurs after 10ms, max value entering sleep mode is 850ms due to housekeeping operation. The host does not have to take any action for this to occur, however, in order to achieve the lowest sleep current, the host needs to shut down its clock to the memory device. In most systems, embedded devices are in sleep mode except when accessed by the host, thus conserving power. When the host is ready to access a memory device in sleep mode, any command issued to it will cause it to exit sleep and respond immediately.

2.6. Sleep (CMD5)

An iNAND device may be switched between a Sleep and a Standby state using the SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized and the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device.

The Vcc power supply may be switched off in Sleep state is to enable even further system power consumption saving.

For additional information please refer JESD84-B451 section number 6.6.28.

2.7. Enhanced Reliable Write

iNAND supports enhanced reliable write as defined in e.MMC 4.51 spec[7].

Enhanced reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing in reliable write, data will remain valid even if a sudden power loss occurs during programming.

2.8. Secure Erase

For backward compatibility reasons, in addition to the standard erase command the iNAND supports the optional Secure Erase command[8].
The Secure Erase command differs from the basic Erase command in that it requires the iNAND to execute the erase operation on the memory array when the command is issued and requires the iNAND and host to wait until the operation is complete before moving to the next iNAND operation.

The secure erase command requires the iNAND to perform a secure purge operation on the erase groups, and copy items identified for erase, in those erase groups .
A purge operation is defined as overwriting addressable locations with a single character and then performing an erase.

This new command meets high security application requirements (e,g, those used by military and government customers) that once data has been erased, it can no longer be retrieved from the device.

[7] For additional information refer to JEDEC Standards No. JESD84-B451

[8] For additional information refer to JEDEC Standards No. JESD84-B451

2.9. Secure Trim

For backward compatibility reasons, iNAND support Secure Trim command. The Secure Trim[9] command is similar to the Secure Erase command but performs a secure purge operation on write blocks instead of erase groups. The size of a write block in the iNAND device is 512B

2.10. Trim

The Trim function is similar to the Erase command but applies the erase operation to write blocks instead of erase groups. The size of a write block in the INAND device is 512B

For additional information on the Trim function, refer to JEDEC standards No. JESD84-B451

2.11. Partition management

The iNAND offers the possibility for the host to configure additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore memory block area scan be classified as follows[10]:

- Factory configuration supplies two boot partitions (refer to section 2.1) implemented as enhanced storage media and one RPMB partitioning of 2MB in size.
- Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group. Size can be programmed once in device life-cycle (one-time programmable).

[9] For additional information refer to JEDEC Standards No. JESD84-B451

[10] For additional information refer to JEDEC Standards No. JESD84-B451

2.12. Device Health

Device Health is SanDisk proprietary feature and is similar to SMART feature of modern hard disks, it provides only vital NAND flash program/erase cycles information in percentage of useful flash life span.

Host can query Device Health information utilizing standard MMC command, CMD_8, to get extended CSD structure. Device health feature will provide % of the wear of the device in 10% fragments.

The following 2 Extended CSD fields will hold the average percentage of usage for an iNAND device. Each one holds a value for of the specified memory types:

- MLC User Area
- SLC Internal memory such as Binary Cache

Name	Field	Size (Byte)	Cell Type	Hex Offset (Byte)	Dec. Offset (Byte)
MLC Device health status	MLC_DEVICE_HEALTH_STATUS	1	R	0x5E	94
SLC Device health status	SLC_DEVICE_HEALTH_STATUS	1	R	0x57	87

2.13. Enhanced Write Protection

To allow the host to protect data against erase or write, the iNAND supports two levels of write protect command[11]:

- The entire iNAND (including the Boot Area Partitions, General Purpose Area Partition, and User Area Partition) may be write-protected by setting the permanent or temporary write protect bits in the CSD.
- Specific segments of the iNAND may be permanently, power-on or temporarily write protected. Segment size can be programmed via the EXT_CSD register.

For additional information please refer JESD84-B451 standard.

2.14. High Priority Interrupt (HPI)

Many operating-systems use demand-paging to launch a process requested by the user. If the host needs to fetch pages while in a middle of a write operation the request will be delayed until the completion of the write command.

[11] For additional information refer to JEDEC Standards No. JESD84-B451

The high priority interrupt (HPI) as defined in JESD84-B451 enables low read latency operation by suspending a lower priority operation before it is actually completed. This mechanism can reduce read latency, in typical condition to below 10msec.

For additional information on the HPI function, refer to JESD84-B451 standard section 6.6.23

2.15. H/W Reset

Hardware reset may be used by host to reset the device, moving the device to a Pre-idle state and disabling the power-on period write protect on blocks that was set as power-on write protect before the reset was asserted. For more information, refer to JESD84-B451 standard.

2.16. DDR I/F

Support DDR signaling to double bus performance. For additional information please refer to JESD84-B451 standard.

3. PRODUCT SPECIFICATIONS

3.1. Typical Power Requirements

Table 3.1 - iNAND Sleep Power Requirements (Ta=25°C@3.3V)

		Max Value	Measurement
Auto Sleep mode		350	uA
Sleep (CMD5 - VCCQ)		200 (Max)	uA
Read	RMS	4GB: 150 8GB: 150	mA
	Peak	4GB: 200 8GB: 250	mA
Write	RMS	4GB: 100 8GB: 150	mA
	Peak	4GB: 200 8GB: 250	mA
VCC (ripple: max, 100mV peak-to-peak) 2.7 V – 3.6 V			

Table 4.2 - iNAND Active Power Requirements RMS VCC / VCCQ (Ta=25°C@3.3V)

Read	RMS VCC	4GB: 40 8GB: 45	mA
	RMS VCCQ	4GB: 105 8GB: 105	mA
Write	RMS VCC	4GB: 40 8GB: 50	mA
	RMS VCCQ	4GB: 40 8GB: 40	mA

Note 1: RMS Current measurements are average over 100 mSecs.

Note 2: Sleep current is measured at room temperature

Note 3: In sleep state, triggered by CMD5, Flash Vcc power supply is switched off

Note 4: Peak current is measured over 3 uSecs.

3.2. Operating Conditions

3.2.1. Operating and Storage Temperature Specifications

Table 5 - Operating and Storage Temperatures

Temperature	Operating	-25° C to 85° C
	Non-Operating: After soldered onto PC Board	-40° C to 85° C

3.2.2. Moisture Sensitivity

The moisture sensitivity level for iNAND is MSL = 3.

3.3. System Performance

All performance values for iNAND in Table 6 were measured under the following conditions:

- Voltage range:

  Core voltage (VCC): 2.7-3.6v

  Host voltage (VCCQ), either: 1.7-1.95v or 2.7-3.6v
- Operating temperature -25° C to 85° C

Table 6a – Sequential System Performance

SKU	Sustained Write	Sustained Read
SDIN7DP2-4G	**12MB/s**	**90MB/s**
SDIN7DP2-8G	**24MB/s**	**90MB/s**

Note 1: Sustained Read & Write performance is measured under DDR Bus width of 8bit at 52Mhz.

Table 7b – Random System Performance

SKU	Sustained Write	Sustained Read
SDIN7DP2-4G	**400 IOPS**	**2500 IOPS**
SDIN7DP2-8G	**500 IOPS**	**2500 IOPS**

Note 2: Sustained Read & Write performance is measured using SanDisk proprietary test environment, w/o FS overhead.

Table 5c - System Timing Performance

Timing	Value
Block Read Access Time (MAX)	100 ms
Block Write Access Time (MAX)	250 ms
CMD1 to Ready after Power-up (MAX)	1000 ms

4. PHYSICAL SPECIFICATIONS

The SanDisk iNAND is a 153 pin, thin fine-pitched ball grid array (BGA). See Figure 2, Figure 3 and Table 8 for physical specifications and dimensions.

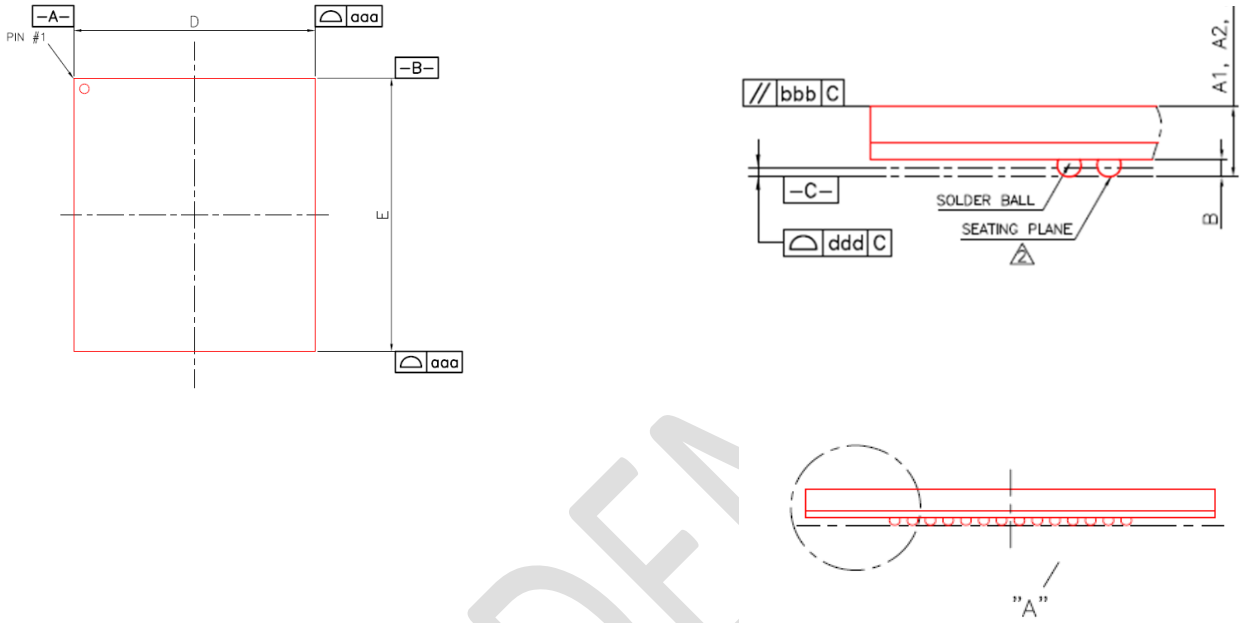
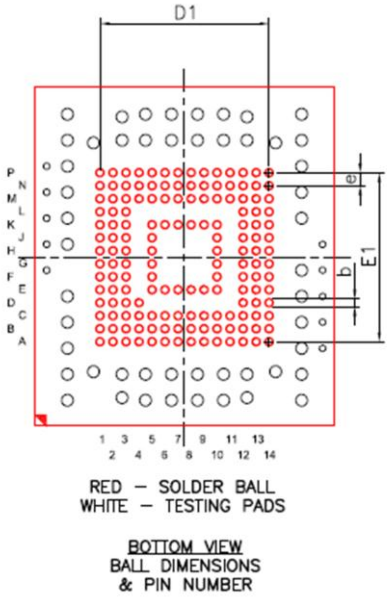


Figure 2- INAND Specification Top and Side View (Detail A)



Legend	
○	Ball
○	Test Pad (for SanDisk internal use only).

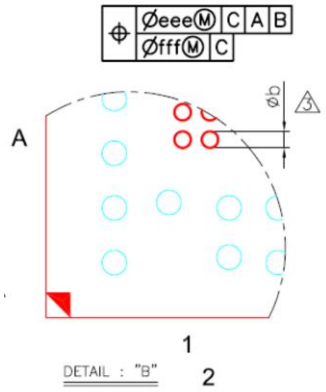


Figure 3- Package Outline Drawing – bottom view

Table 8 - iNAND Package Specification

153 ball		Dimension in millimeters			Dimension in inches		
Package Size	**Symbol**	**Minimum**	**Nominal**	**Maximum**	**Minimum**	**Nominal**	**Maximum**
11.5X13X1.0	A1	---	---	1.00	---	---	0.039
All	B	0.17	0.22	0.27	0.007	0.009	0.011
All	D	11.40	11.50	11.60	0.449	0.453	0.457
All	E	12.90	13.00	13.10	0.508	0.512	0.516
All	D1	---	6.50	---	---	0.256	---
All	E1	---	6.50	---	---	0.256	---
All	e	---	0.50	---	---	0.020	---
All	B	0.25	0.30	0.35	0.010	0.012	0.014
All	Aaa	0.10	0.004				
All	Bbb	0.10			0.004		
All	Ddd	0.08			0.003		
All	MD/ME	14/14			14/14		

5. INTERFACE DESCRIPTION

5.1. MMC I/F Ball Array 153 ball

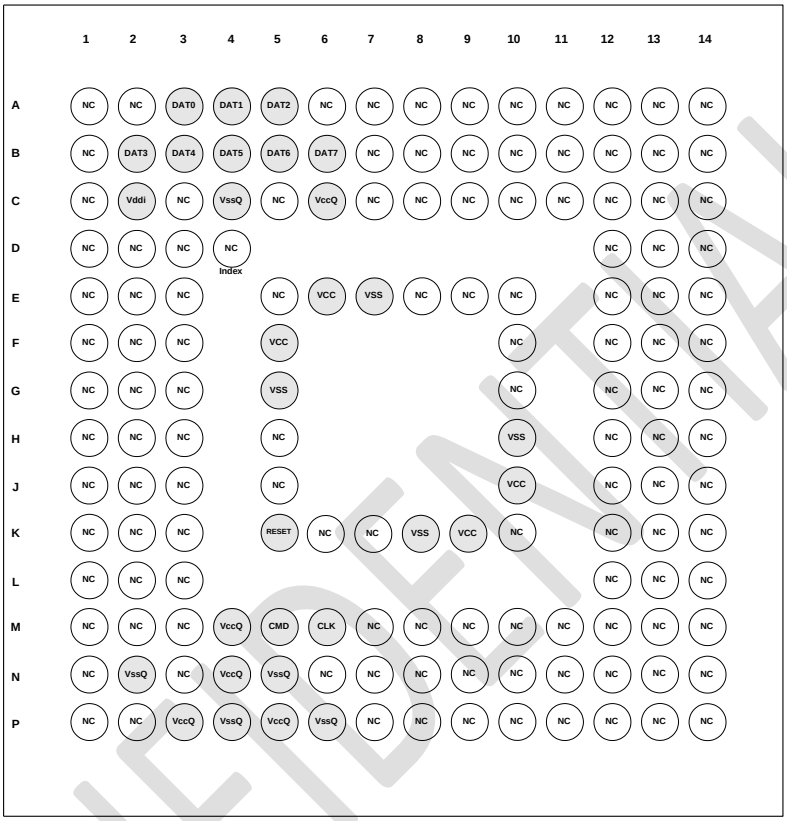


Figure 4 - 153 balls - Ball Array (Top View)

5.2. Pins and Signal Description 153 balls

Table 7a contains the SanDisk iNAND *Ulta*, with MMC interface, functional pin assignment.

Table 7a – Functional Pin Assignment

Ball No.	Ball Signal	Type	Description
A3	DAT0	I/O	Data I/O: Bidirectional channel used for data transfer
A4	DAT1		
A5	DAT2		
B2	DAT3		
B3	DAT4		
B4	DAT5		
B5	DAT6		
B6	DAT7		
M5	CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers.
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
K5	RST_n		Hardware Reset
E6	VCC	Supply	Flash I/O and memory power supply
F5	VCC		
J10	VCC		
K9	VCC		
C6	VCCQ	Supply	Memory controller core and MMC I/F I/O power supply
M4	VCCQ		
N4	VCCQ		
P3	VCCQ		
P5	VCCQ		
E7	VSS	Supply	Flash I/O and memory ground connection
G5	VSS		
H10	VSS		
K8	VSS		
C4	VSSQ		Memory controller core and MMC I/F ground connection
N2	VSSQ		
N5	VSSQ		
P4	VSSQ		
P6	VSSQ		
C2	VDDi		Internal power node. Connect 0.1uF capacitor from VDDi to ground

Note: All other pins are not connected [NC] and can be connected to GND or left floating.

5.3. iNAND Registers

5.3.1. OCR Register

Value: 0xC0FF8080

Note: Bit 30 is set because the device is High Capacity; bit 31 will be set only when the device is ready

Parameter	OCR slice	Description	Value	**Width**
Access Mode	[30:29]	Access mode	10b	2
	[23:15]	VDD: 2.7 - 3.6 range	111111111b	9
	[14:8]	VDD: 2.0 - 2.6 range	0000000b	7
	[7]	VDD: 1.7 - 1.95 range	1b	1

5.3.2. CID Register

Parameter	**CID slice**	**Description**	**Value**	**Width**
MID	[127:120]	Manufacturer ID	45h	8
CBX	[113:112]	Device BGA	01h	2
OID	[111:104]	OEM/Application ID	0000h	8
PNM	[103:56]	Product name	4GB: 53454d313647h ("SEM04G") 8GB: 53454d333247h ("SEM08G")	48
PRV	[55:48]	Product revision	Counter to indicate FW revision	8
PSN	[47:16]	Product serial number	Random by Production	32
MDT[12]	[15:8]	Manufacturing date	month, year	8
CRC	[7:1]	CRC7 checksum	0000000b	7

5.3.3. DSR Register

Parameter	**DSR slice**	**Description**	**Value**	**Width**
RSRVD	[15:8]	Reserved	04h	8
RSRVD	[7:0]	Reserved	04h	8

DSR is not implemented; in case of read, value of 0x0404 will be returned.

[12] Compatible to JESD84-B451

5.3.4. CSD Register

Parameter	CSD Slice	Description	Value	Width
CSD_STRUCTURE	[127:126]	CSD structure	11b	3
SPEC_VERS	[125:122]	System specification version	0100b	4
TAAC	[119:112]	Data read access-time 1	0Fh	8
NSAC	[111:104]	Data read access-time 2 in CLK cycles (NSAC*100)	00h	8
TRAN_SPEED	[103:96]	Max. bus clock frequency	32h	8
CCC	[95:84]	Device command classes	0F5h	12
READ_BL_LEN	[83:80]	Max. read data block length	9h	4
READ_BL_PARTIAL	[79:79]	Partial blocks for read allowed	0b	1
WRITE_BLK_MISALIGN	[78:78]	Write block misalignment	0b	1
READ_BLK_MISALIGN	[77:77]	Read block misalignment	0b	1
DSR_IMP	[76:76]	DSR implemented	0b	1
C_SIZE	[73:62]	Device size	FFFh	12
VDD_R_CURR_MIN	[61:59]	Max. read current @ VDD min	111b	3
VDD_R_CURR_MAX	[58:56]	Max. read current @ VDD max	111b	3
VDD_W_CURR_MIN	[55:53]	Max. write current @ VDD min	111b	3
VDD_W_CURR_MAX	[52:50]	Max. write current @ VDD max	111b	3
C_SIZE_MULT	[49:47]	Device size multiplier	111b	3
ERASE_GRP_SIZE	[46:42]	Erase group size	11111b	5
ERASE_GRP_MULT	[41:37]	Erase group size multiplier	11111b	5
WP_GRP_SIZE	[36:32]	Write protect group size	11111b	5
WP_GRP_ENABLE	[31:31]	Write protect group enable	1b	1
DEFAULT_ECC	[30:29]	Manufacturer default	00b	2
R2W_FACTOR	[28:26]	Write speed factor	10b	3
WRITE_BL_LEN	[25:22]	Max. write data block length	9h	4
WRITE_BL_PARTIAL	[21:21]	Partial blocks for write allowed	0b	1
CONTENT_PROT_APP	[16:16]	Content protection application	0b	1
FILE_FORMAT_GRP	[15:15]	File format group	0b	1
COPY	[14:14]	Copy flag (OTP)	1b	1
PERM_WRITE_PROTECT	[13:13]	Permanent write protection	0b	1
TMP_WRITE_PROTECT	[12:12]	Temporary write protection	0b	1
FILE_FORMAT	[11:10]	File format	00b	2
ECC	[9:8]	ECC code	00b	2
CRC	[7:1]	Calculated CRC	0000000b	7

5.3.5. EXT_CSD Register

Parameter	ECSD slice [bytes]	Description	Value
S_CMD_SET	[504]	Supported Command Sets	1h
HPI_FEATURES	[503]	HPI Features	1h
BKOPS_SUPPORT	[502]	Background operations support	1h
MAX_PACKED_READS	[501]	Max packed read commands	3Fh
MAX_PACKED_WRITES	[500]	Max packed write commands	3Fh
DATA_TAG_SUPPORT	[499]	Data Tag Support	1h
TAG_UNIT_SIZE	[498]	Tag Unit Size	3h
TAG_RES_SIZE	[497]	Tag Resources Size	3h
CONTEXT_CAPABILITIES	[496]	Context management capabilities	5h
LARGE_UNIT_SIZE_M1	[495]	Large Unit size	0h
EXT_SUPPORT	[494]	Extended partitions attribute support	0h
CACHE_SIZE	[252:249]	Cache size	0000h
GENERIC_CMD6_TIME	[248]	Generic CMD6 timeout	19h
POWER_OFF_LONG_TIME	[247]	Power off notification(long) timeout	64h
BKOPS_STATUS	[246]	Background operations status	Default = 0h Updated in Run time
CORRECTLY_PRG_SECTORS_NUM	[245:242]	Number of correctly programmed sectors	Default = 0h Updated in Run time
INI_TIMEOUT_AP	[241]	1st Initialization time after partitioning	Ah
PWR_CL_DDR_52_360	[239]	Power class for 52MHz, DDR at 3.6V	4GB = 0h 8GB = 22h
PWR_CL_DDR_52_195	[238]	Power class for 52MHz, DDR at 1.95V	0h
PWR_CL_200_195	[237]	Power class for 200MHz at 3.6V	0h
PWR_CL_200_130	[236]	Power class for 200MHz, at 1.95V	0h
MIN_PERF_DDR_W_8_52	[235]	Minimum Write Performance for 8bit at 52MHz in DDR mode	0h
MIN_PERF_DDR_R_8_52	[234]	Minimum Read Performance for 8bit at 52MHz in DDR mode	0h
TRIM _MULT	[232]	TRIM Multiplier	Eh
SEC_FEATURE_SUPPORT	[231]	Secure Feature support	55h
SEC_ERASE_MULT	[230]	Secure Erase Multiplier	44h
SEC_TRIM_MULT	[229]	Secure TRIM Multiplier	44h
BOOT_INFO	[228]	Boot Information	7h
BOOT_SIZE_MULT	[226]	Boot partition size	10h
ACCESS_SIZE	[225]	Access size	8h
HC_ERASE_GROUP_SIZE	[224]	High Capacity Erase unit size	Table 8

Parameter	ECSD slice [bytes]	Description	Value
ERASE_TIMEOUT_MULT	[223]	High capacity erase time out	Eh
REL_WR_SEC_C	[222]	Reliable write sector count	1h
HC_WP_GRP_SIZE	[221]	High capacity write protect group size	Table 8
S_C_VCC	[220]	Sleep current [VCC]	8h
S_C_VCCQ	[219]	Sleep current [VCCQ]	7h
S_A_TIMEOUT	[217]	Sleep/Awake time out	13h
SEC_COUNT	[215:212]	Sector count	Table 9
MIN_PERF_W_8_52	[210]	Minimum Write Performance for 8bit @52MHz	Ah
MIN_PERF_R_8_52	[209]	Minimum Read Performance for 8bit @52MHz	Ah
MIN_PERF_W_8_26_4_52	[208]	Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_R_8_26_4_52	[207]	Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_W_4_26	[206]	Minimum Write Performance for 4bit @26MHz	Ah
MIN_PERF_R_4_26	[205]	Minimum Read Performance for 4bit @26MHz	Ah
PWR_CL_26_360	[203]	Power Class for 26MHz @ 3.6V	4GB: 00h 8GB: 22h
PWR_CL_52_360	[202]	Power Class for 52MHz @ 3.6V	4GB: 00h 8GB: 22h
PWR_CL_26_195	[201]	Power Class for 26MHz @ 1.95V	0h
PWR_CL_52_195	[200]	Power Class for 52MHz @ 1.95V	0h
PARTITION_SWITCH_TIME	[199]	Partition switching timing	3h
OUT_OF_INTERRUPT_TIME	[198]	Out-of-interrupt busy timing	19h
DRIVER_STRENGTH	[197]	I/O Driver Strength	1h
DEVICE_TYPE	[196]	Device Type	7h
CSD_STRUCTURE	[194]	CSD Structure Version	2h
EXT_CSD_REV	[192]	Extended CSD Revision	6h
CMD_SET	[191]	Command Set	Default = 0h Updated in Run time
CMD_SET_REV	[189]	Command Set Revision	0h
POWER_CLASS	[187]	Power Class	4GB = 0h 8GB = 2h
HS_TIMING	[185]	High Speed Interface Timing	Default = 0h Updated in Run time
BUS_WIDTH	[183]	Bus Width Mode	Default = 0h

Parameter	ECSD slice [bytes]	Description	Value
			Updated in Run time
ERASE_MEM_CONT	[181]	Content of explicit erased memory range	0h
PARTITION_CONFIG	[179]	Partition Configuration	Default = 0h Updated in Run time
BOOT_CONFIG_PROT	[178]	Boot config protection	Default = 0h Updated in Run time
BOOT_BUS_CONDITIONS	[177]	Boot bus width1	Default = 0h Updated in Run time
ERASE_GROUP_DEF	[175]	High-density erase group definition	Default = 0h Updated in Run time
BOOT_WP_STATUS	[174]	Boot write protection status registers	Default = 0h Updated in Run time
BOOT_WP	[173]	Boot area write protect register	0h
USER_WP	[171]	User area write protect register	0h
FW_CONFIG	[169]	FW Configuration	0h
RPMB_SIZE_MULT	[168]	RPMB Size	10h
WR_REL_SET	[167]	Write reliability setting register	1Fh
WR_REL_PARAM	[166]	Write reliability parameter register	5h
SANITIZE_START	[165]	Start Sanitize operation	Default = 0h Updated in Run time
BKOPS_START	[164]	Manually start background operations	Default = 0h Updated in Run time
BKOPS_EN	[163]	Enable background operations handshake	0h
RST_n_FUNCTION	[162]	H/W reset function	Default = 0h Updated by the host
HPI_MGMT	[161]	HPI management	Default = 0h Updated by the host
PARTITIONING SUPPORT	[160]	Partitioning support	1h
MAX_ENH_SIZE_MULT	[159:157]	Max Enhanced Area Size	N/A
PARTITIONS_ATTRIBUTE	[156]	Partitions Attribute	Default = 0h Updated by the host
PARTITION_SETTING_ COMPLETED	[155]	Partitioning Setting	Default = 0h Updated by the host
GP_SIZE_MULT	[154:143]	General Purpose Partition Size	0h
ENH_SIZE_MULT	[142:140]	Enhanced User Data Area Size	0h
ENH_START_ADDR	[139:136]	Enhanced User Data Start Address	0h

Parameter	ECSD slice [bytes]	Description	Value
SEC_BAD_BLK_MGMNT	[134]	Bad Block Management mode	0h
TCASE_SUPPORT	[132]	Package Case Temperature is controlled	0h
PERIODIC_WAKEUP	[131]	Periodic Wake-up	0h
PROGRAM_CID_CSD_DDR_SUPPORT	[130]	Program CID/CSD in DDR mode support	1h
VENDOR_SPECIFIC_FIELD	[127:64]	Vendor Specific Fields	reserved
NATIVE_SECTOR_SIZE	[63]	Native sector size	0h
USE_NATIVE_SECTOR	[62]	Sector size emulation	0h
DATA_SECTOR_SIZE	[61]	Sector size	0h
INI_TIMEOUT_EMU	[60]	1st initialization after disabling sector size emulation	0h
CLASS_6_CTRL	[59]	Class 6 commands control	0h
DYNCAP_NEEDED	[58]	Number of addressed group to be Released	0h
EXCEPTION_EVENTS_CTRL	[57:56]	Exception events control	0h
EXCEPTION_EVENTS_STATUS	[55:54]	Exception events status	0h
EXT_PARTITIONS_ATTRIBUTE	[53:52]	Extended Partitions Attribute	0h
CONTEXT_CONF	[51:37]	Context configuration	Default = 0h Updated in Run time
PACKED_COMMAND_STATUS	[36]	Packed command status	Default = 0h Updated in Run time
PACKED_FAILURE_INDEX	[35]	Packed command failure index	Default = 0h Updated in Run time
POWER_OFF_NOTIFICATION	[34]	Power Off Notification	Default = 0h Updated in Run time
CACHE_CTRL	[33]	Control to turn the Cache ON/OFF	0h
FLUSH_CACHE	[32]	Flushing of the cache	0h

The following table shows the capacity available for user data for the various device capacities:

Table 9: Capacity for User Data*

Capacity	LBA [Hex]	LBA [Dec]	Capacity [Bytes]
SDIN7DP2-4G	0x760000	7,733,248	3,959,422,976
SDIN7DP2-8G	0xE90000	15,269,888	7,818,182,656

.

Table 10: Write protect group size

SKU	HC_ERASE_GROUP_SIZE	HC_WP_GRP_SIZE	Erase Unit Size [MB]	Write Protect Group Size [MB]
SDIN7DP2-4G	4h	4h	2MB	8MB
SDIN7DP2-8G	4h	8h	2MB	16MB

6. POWER DELIVERY AND CAPACITOR SPECIFICATIONS

6.1. SanDisk iNAND UltraPower Domains

SanDisk iNAND Ultra has three power domains assigned to VCCQ, VCC and VDDi, as shown in Table 11.

Table 11 - Power Domains

Pin	Power Domain	Comments
VCCQ	Host Interface	Supported voltage ranges:
		High Voltage Region: 3.3V (nominal)
		Low Voltage Region: 1.8V (nominal)
VCC	Memory	Supported voltage range:
		High Voltage Region: 3.3V (nominal)
VDDi	Internal	VDDi is the internal regulator connection to an external decoupling capacitor.

6.2. Capacitor Connection Guidelines

6.2.1. VDDi Connections

The VDDi (C2/K2) ball must only be connected to an external capacitor that is connected to VSS. This signal may not be left floating. The capacitor's specifications and its placement instructions are detailed below.

The capacitor is part of an internal voltage regulator that provides power to the controller.

Caution: Failure to follow the guidelines below, or connecting the VDDi ball to any external signal or power supply, may cause the device to malfunction.

The trace requirements for the VDDi (C2/K2) ball to the capacitor are as follows:

- Resistance: <2 ohm
- Inductance: <5 nH

The capacitor requirements are as follows:

- Capacitance: >=0.1 uF
- Voltage Rating: >=6.3 V
- Dielectric: X7R or X5R

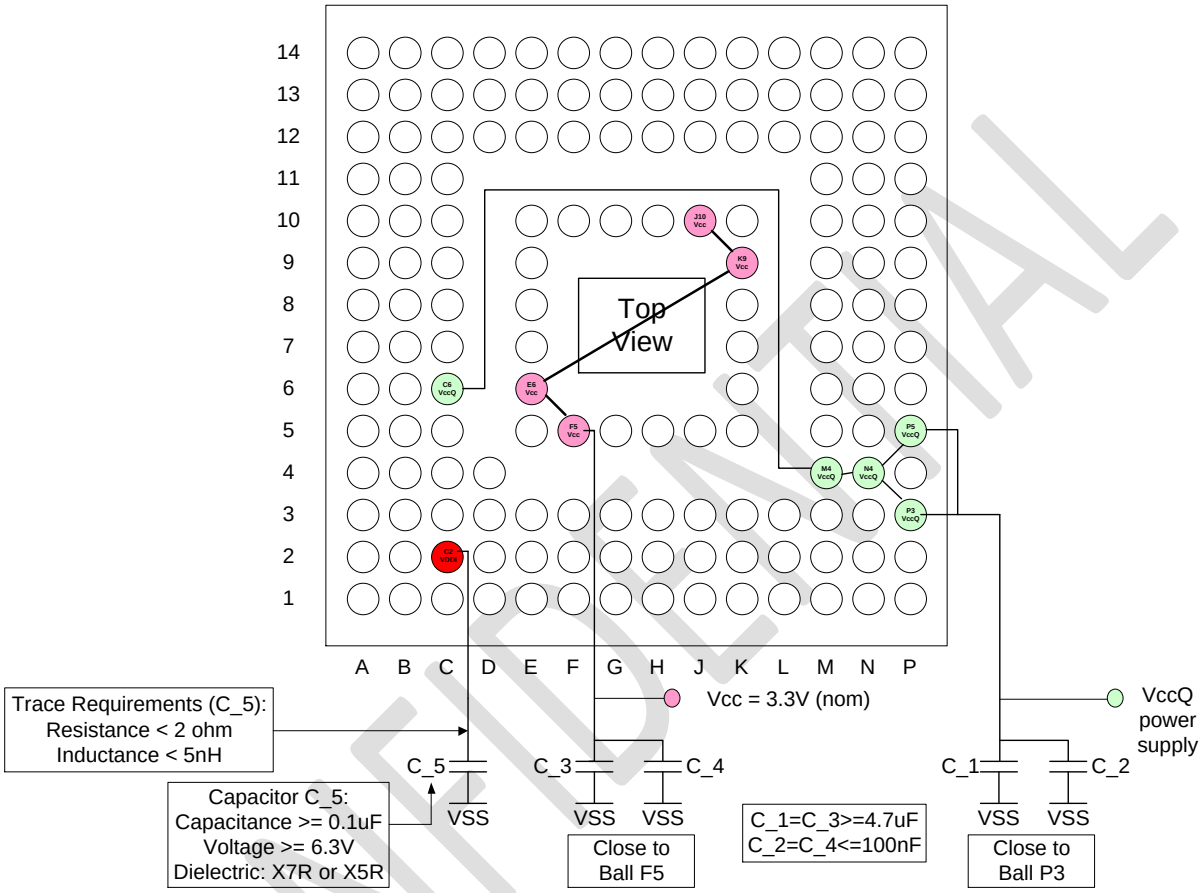
6.2.2. VCC and VCCQ Connections

- All VCC balls should be connected to a 3.3V supply
- All VCCQ balls should be connected either to a 3.3V or 1.8V supply

SanDisk recommends providing separate bypass capacitors for each power domain as shown in Figure 5.

Note: Signal routing in the diagram is for illustration purposes only and the final routing depends on your PCB layout. Also, for clarity, the diagram does not show the VSS connection. All balls marked VSS should be connected to a ground (GND) plane.

Figure 5- Recommended Power Domain Connections



7. MARKING

First row: Simplified SanDisk Logo

Second row: Sales item P/N

Third row: Country of origin i.e. 'TAIWAN' or 'CHINA'

* No ES marking for product in mass production.

Fourth row: Y- Last digit of year

WW- Work week

D- A day within the week.

MTLLXXX – Internal use

2D barcode: Store the 10 Digital unique ID information as reflected in the fourth row.

Figure 6: Product marking

8. ORDERING INFORMATION

Table 12 – Ordering Information

Capacity	Technology	Part Number	Samples Part Number	Package
4GB	X2	SDIN7DP2-4G	SDIN7DP2-4G-Q	11.5mm x 13mm x 1.0mm
8GB	X2	SDIN7DP2-8G	SDIN7DP2-8G-Q	11.5mm x 13mm x 1.0mm

Note 1: Suffix "T" added to the P/N indicates tape/reel. For example, SDIN7DP2-8G would become SDIN7DP2-8G-T. The default P/Ns in Table 10 are shipped in trays.

Note 2: Optional Customer Code in case applicable will be added at the end of the part number. For example SDIN7DP2-8G-999 or SDIN7DP2-8G-999Q

HOW TO CONTACT US

USA
SanDisk Corporation, Corporate Headquarters.
951 SanDisk Drive
Milpitas, CA 95035-7933
Phone: +1-408-801-1000
Fax: +1-408-801-8657

Europe
SanDisk IL Ltd.
7 Atir Yeda St.
Kfar Saba 44425, Israel
Phone: +972-9-764-5000
Fax: +972-3-548-8666

Japan
SanDisk Limited (Japan)
Shinagawa Tokyu Bldg., 3F
1-6-31, Konan, Minato-ku
Tokyo, Japan 108-0075
+81-3-4334-7110 (OEM Sales)

Korea
SanDisk Korea Ltd.
6F Samhwa bldg,
Yangjae-dong 14-8,
Seocho-gu, Seoul 137-130, Korea
Phone:+82-2-3452-9079
Fax: +82-2-3452-9145

Taiwan
SanDisk Asia Ltd.
37F, Taipei 101 Tower, No 7,
Xinyi Rd, Section 5.
Taipei, Taiwan, 110
Tel: +886-2-8758-2966
Fax: +886-2-8758-2999

China
SanDisk China Ltd.
Room 121-122
Bldg. 2, International Commerce & Exhibition Ctr.
Hong Hua Rd. Futian Free Trade Zone
Shenzhen, China
Phone: +86-755-8348-5218
Fax: +86-755-8348-5418

Internet
http://www.SanDisk.com

Sales and Technical Information
techsupport@SanDisk.com